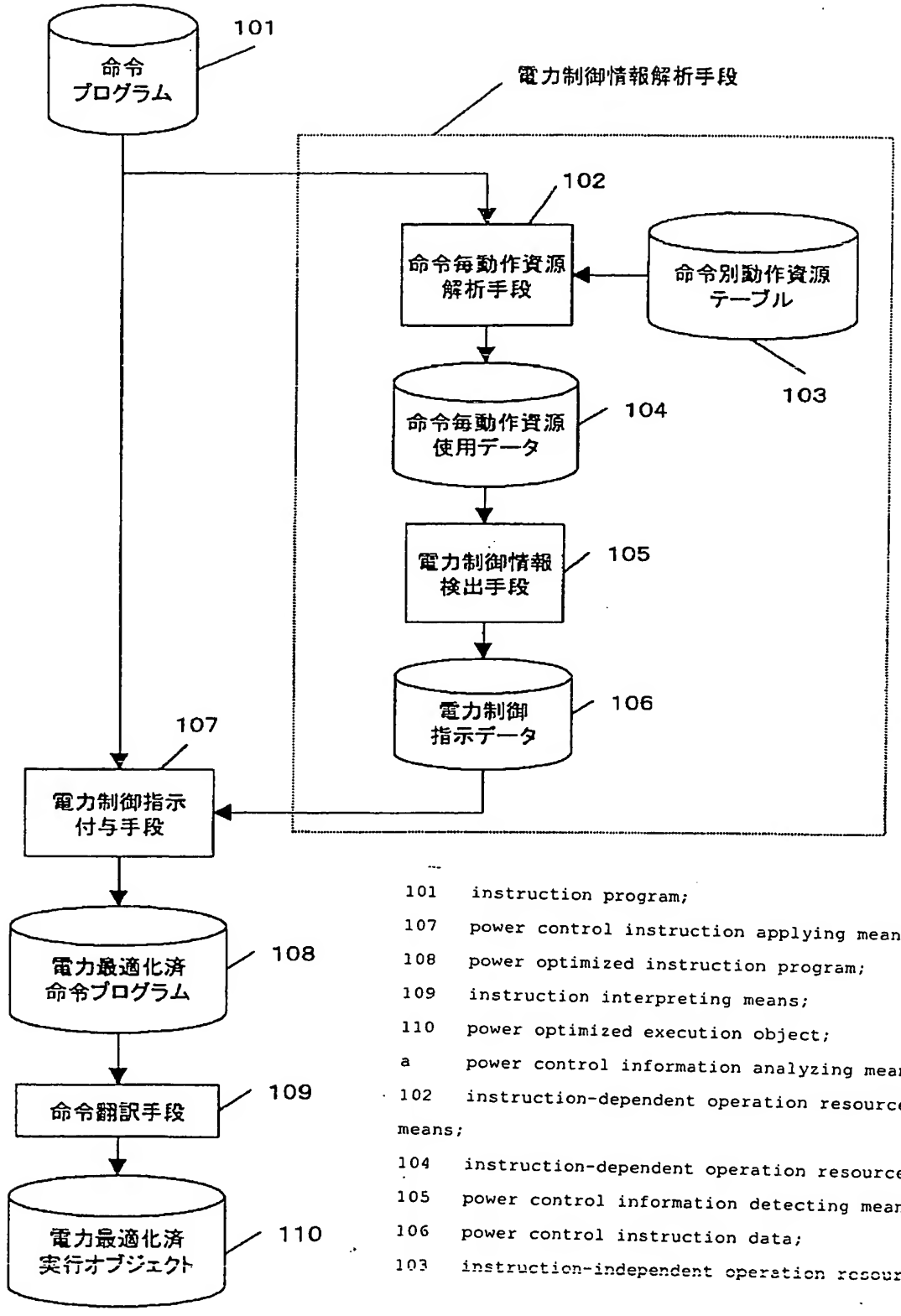
Fig.1



101 instruction program;

107 power control instruction applying means;

108 power optimized instruction program;

109 instruction interpreting means;

110 power optimized execution object;

a power control information analyzing means;

102 instruction-dependent operation resource analyzing means;

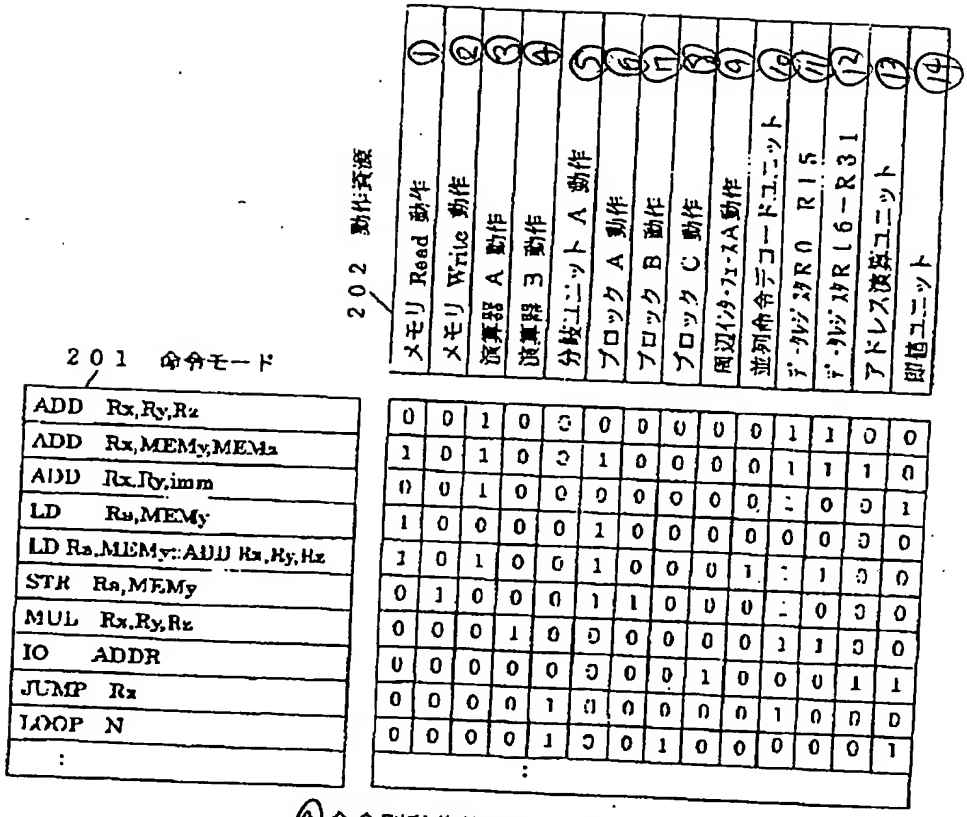
104 instruction-dependent operation resource use data;

105 power control information detecting means;

106 power control instruction data;

103 instruction-independent operation resource table;

Fig.2



④命令別動作資源テーブル

201 instruction mode;

④ instruction-independent operation resource table;

202 operation resource;

① memory Read operation;

② memory Write operation;

③ calculator A operation;

④ calculator B operation;

⑤ branch unit A operation;

⑥ block A operation;

⑦ block B operation;

⑧ block C operation;

⑨ peripheral interface A operation;

⑩ parallel instruction decode unit;

⑪ data register R0 to R15;

⑫ data register R16 to R31;

⑬ address calculation unit;

⑭ threshold value unit;

Fig.3

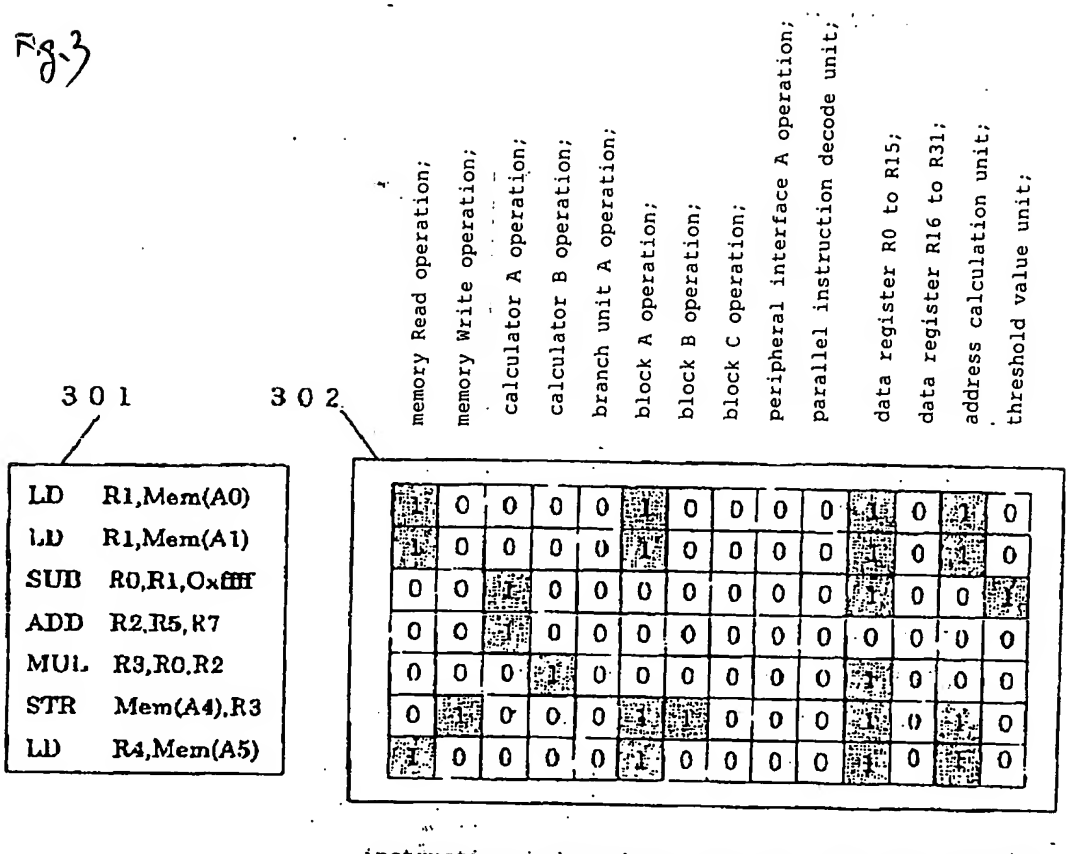

301
302
LD R1,Mem(A0)
LD R1,Mem(A1)
SUB R0,R1,Oxffff
ADD R2,R5,R7
MUL R3,R0,R2
STR Mem(A4),R3
LD R4,Mem(A5)
memory Read operation;
memory Write operation;
calculator A operation;
calculator B operation;
branch unit A operation;
block A operation;
block B operation;
block C operation;
peripheral interface A operation;
parallel instruction decode unit;
data register R0 to R15;
data register R16 to R31;
address calculation unit;
threshold value unit;
instruction-independent operation resource use data;

Fig.4

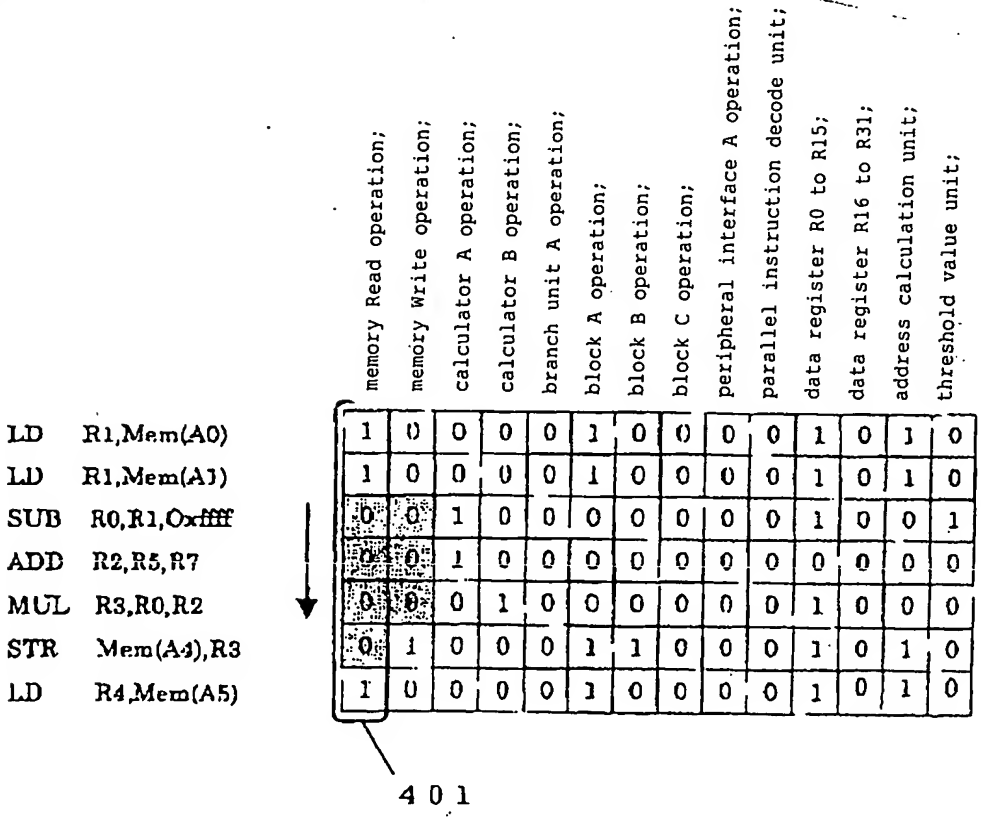

LD R1,Mem(A0)
LD R1,Mem(A1)
SUB R0,R1,Oxffff
ADD R2,R5,R7
MUL R3,R0,R2
STR Mem(A4),R3
LD R4,Mem(A5)
memory Read operation;
memory Write operation;
calculator A operation;
calculator B operation;
branch unit A operation;
block A operation;
block B operation;
block C operation;
peripheral interface A operation;
parallel instruction decode unit;
data register R0 to R15;
data register R16 to R31;
address calculation unit;
threshold value unit;
401

Fig.5

```
LD    R1,Mem(A0)
LD    R1,Mem(A1)
SET PCR, #Memory_Read_Stop
SUB   R0,R1,0xffff
ADD   R2,R5,R7
MUL   R3,R0,R2
STR   Mem(A4),R3
CLR PCR, #Memory_Read_Stop
LD    R4,Mem(A5)
```

Fig.6

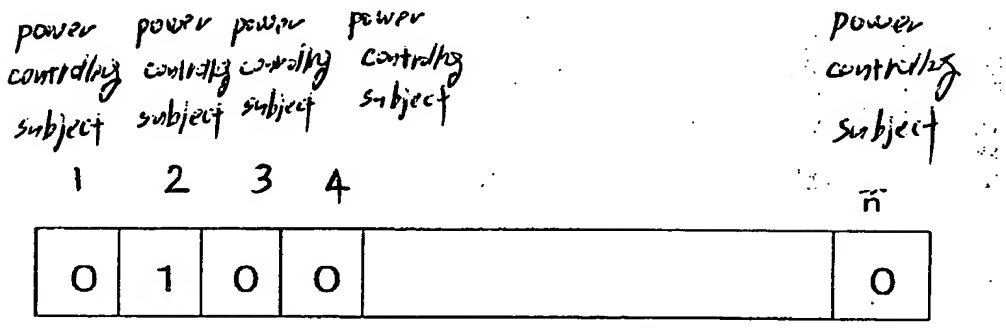
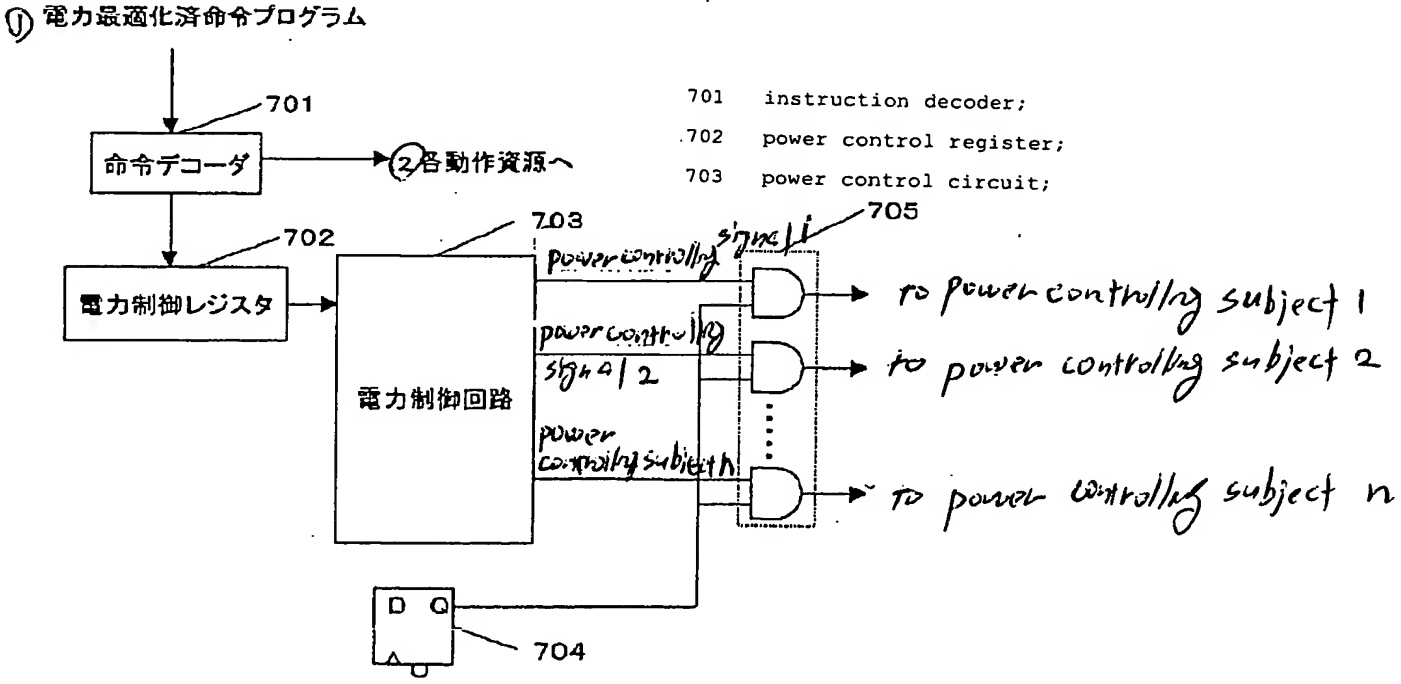


Fig.7



① power optimized instruction program;
② to respective operation resources;

701 instruction decoder;
702 power control register;
703 power control circuit;

Fig.8

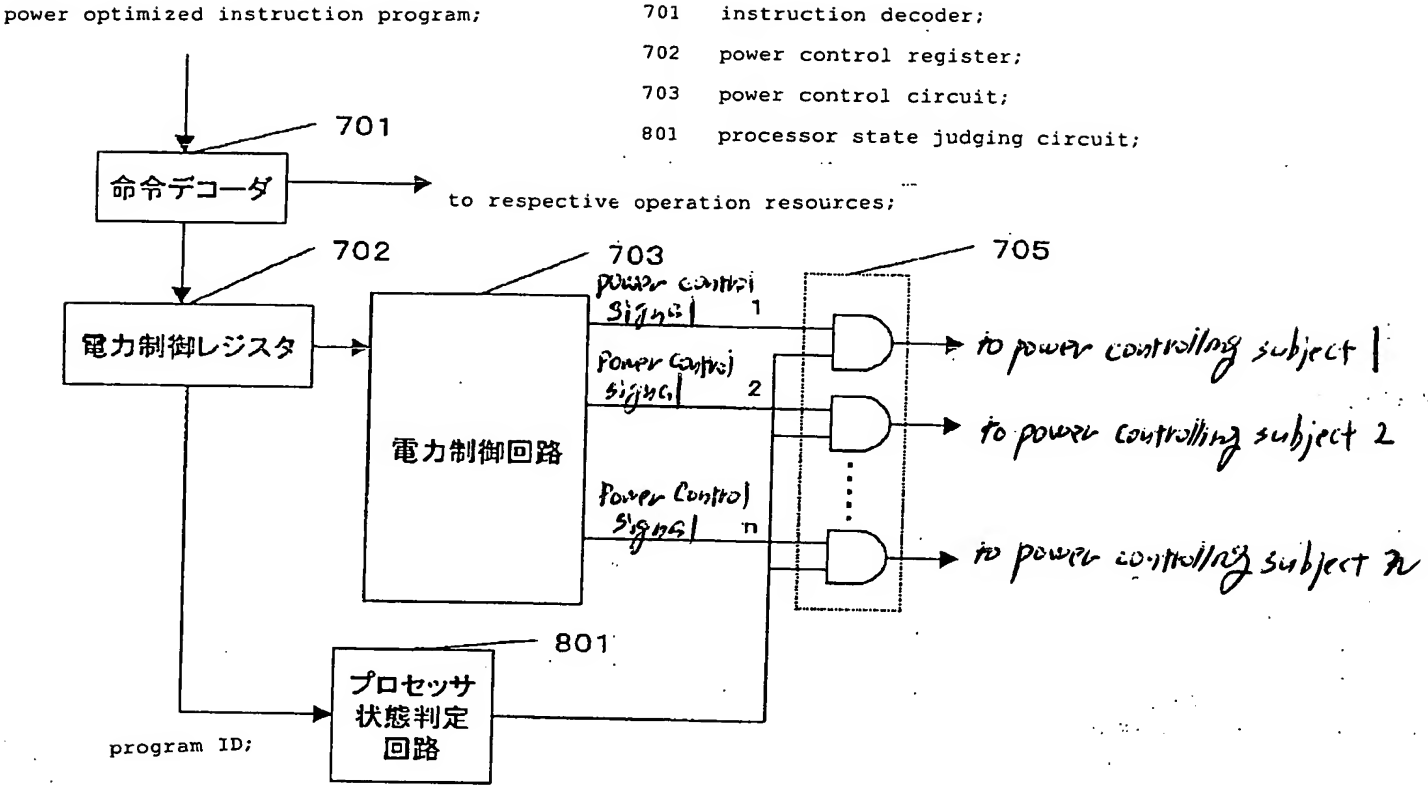


Fig.9

①プログラムID	②電力制御機能ON／OFF
ID1	ON
ID2	ON
ID3	OFF
ID4	ON

① program ID;

② power control function ON/OFF;

Fig.10

```
data_a = data_b*1.75;
data_c = func_calc_d( in1, in2, in3 );

if ( cond_k = = 1 ){ adrs1 = adrs1 + 8; }

#pragma POWER_CONT_ON_Level1
for ( i=0 ; i<256 ; i ++ ){
  out_sum = out_sum * data_c[adrs1]
}
#pragma POWER_CONT_OFF

if ( out_sum > 24 ){ adrs1 = adrs1 + 32; }
```

Fig.11

①レベル	② 制御内容
Level 0	③命令置換によって停止可能な動作資源のみ検出
Level 1	④10区間以上動作しない動作資源を検出
Level 2	⑤ 5区間以上動作しない動作資源を検出
Level 3	⑥ 3区間以上動作しない動作資源を検出

① level;

② control content;

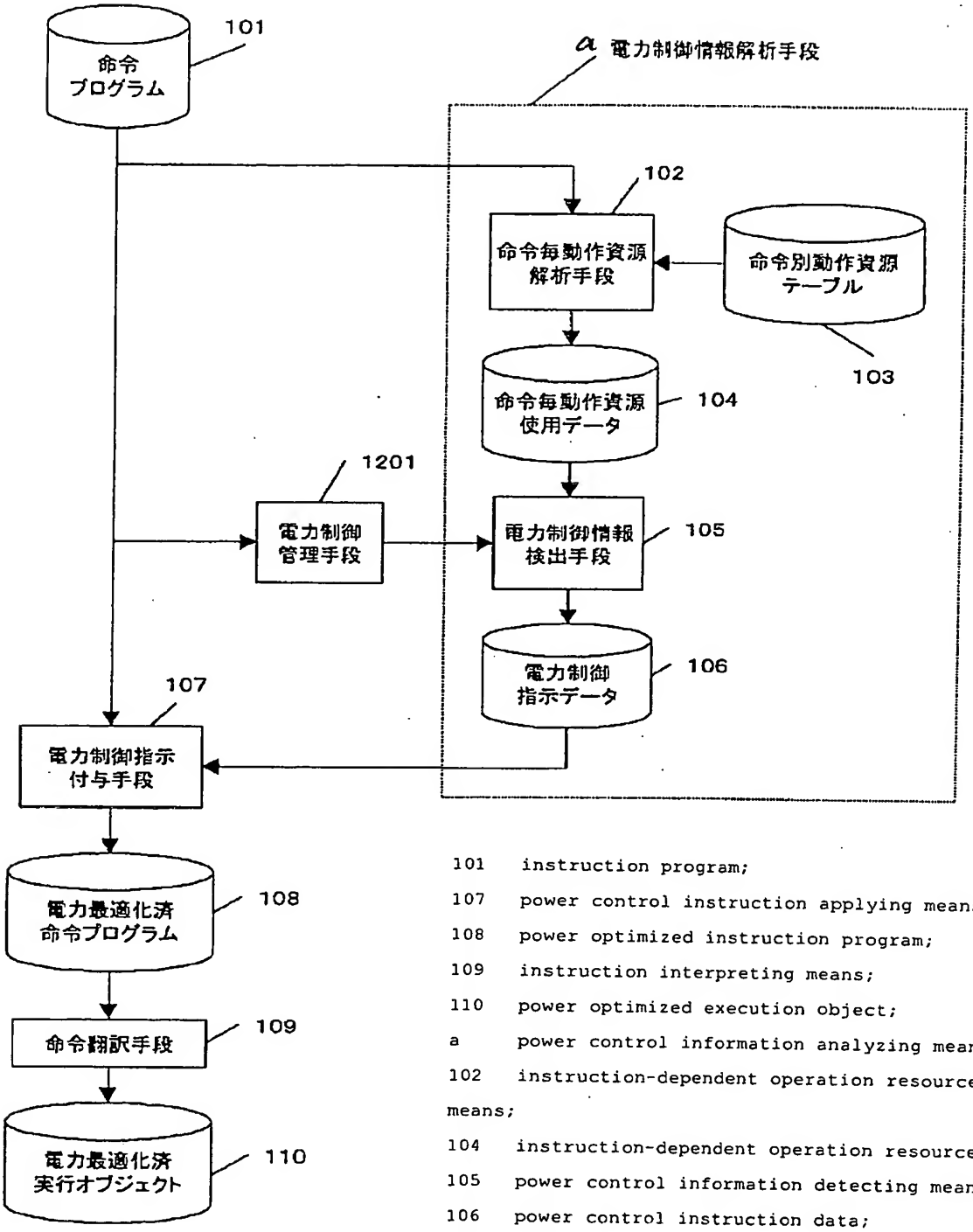
③ only operation resource which can be stopped is detected by replacing instructions;

④ operation resource which is not actuated for 10, or more sections is detected;

⑤ operation resource which is not actuated for 5, or more sections is detected;

⑥ operation resource which is not actuated for 3, or more sections is detected;

Fig.12



101 instruction program;

107 power control instruction applying means;

108 power optimized instruction program;

109 instruction interpreting means;

110 power optimized execution object;

a power control information analyzing means;

102 instruction-dependent operation resource analyzing means;

104 instruction-dependent operation resource use data;

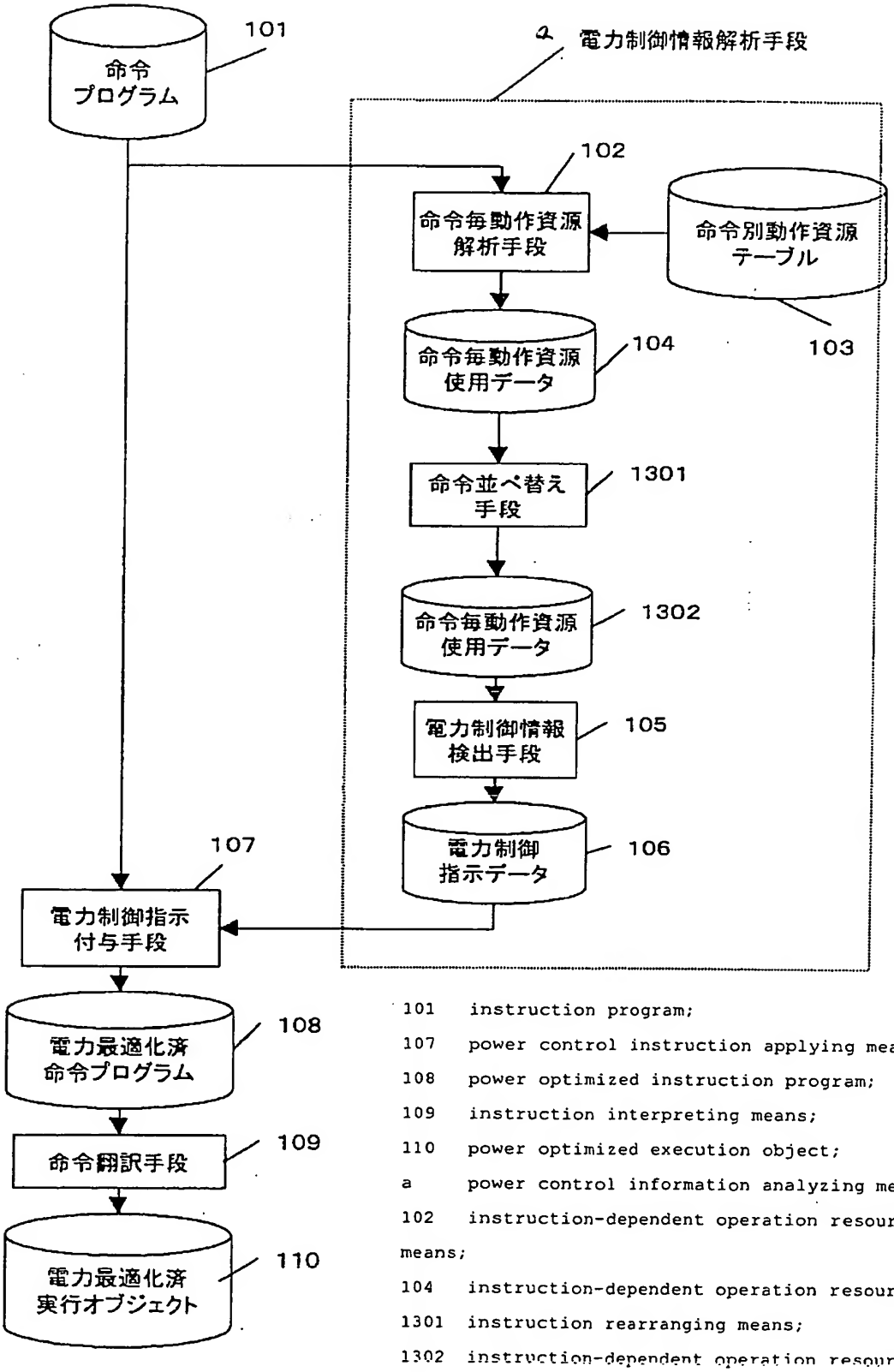
105 power control information detecting means;

106 power control instruction data;

103 instruction-independent operation resource table;

1201 power control managing means;

Fig.13



101 instruction program;

107 power control instruction applying means;

108 power optimized instruction program;

109 instruction interpreting means;

110 power optimized execution object;

a power control information analyzing means;

102 instruction-dependent operation resource analyzing means;

104 instruction-dependent operation resource use data;

1301 instruction rearranging means;

1302 instruction-dependent operation resource use data;

105 power control information detecting means;

106 power control instruction data;

103 instruction-independent operation resource table;

Fig.19.

		①メモリRead動作	②メモリWrite動作	③演算器A動作	④演算器B動作	⑤分岐ユニットA動作	⑥ブロックA動作	⑦ブロックB動作	⑧ブロックC動作	⑨周辺インターフェース動作	⑩並列命令デコードユニット	⑪データレジスタR0−R15	⑫データレジスタR16−R31	⑬アドレス演算ユニット	⑭即値ユニット
MOV	R0, 0X00aa	0	0	1	0	0	0	0	0	0	0	1	0	0	1
ADD	R5, R5, R0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
LD	R1, Mem(A1)	1	0	0	0	0	1	0	0	0	0	1	0	1	0
SUB	R0, R1, 0X0fff	0	0	1	0	0	0	0	0	0	0	1	0	0	1
LD	R7, Mem(A0)	1	0	0	0	0	1	0	0	0	0	1	0	1	0
ADD	R2, R5, R7	0	0	1	0	0	0	0	0	0	0	0	0	0	0
MUL	R3, R0, R2	0	0	0	1	0	0	0	0	0	0	1	0	0	0
STR	Mem(A4), R3	0	1	0	0	0	1	1	0	0	0	1	0	1	0

1 memory Read operation;
2 memory Write operation;
3 calculator A operation;
4 calculator B operation;
5 branch unit A operation;
6 block A operation;
7 block B operation;
8 block C operation;
9 peripheral interface A operation;
10 parallel instruction decode unit;
11 data register R0 to R15;
12 data register R16 to R31;
13 address calculation unit;
14 threshold value unit;

Fig.15

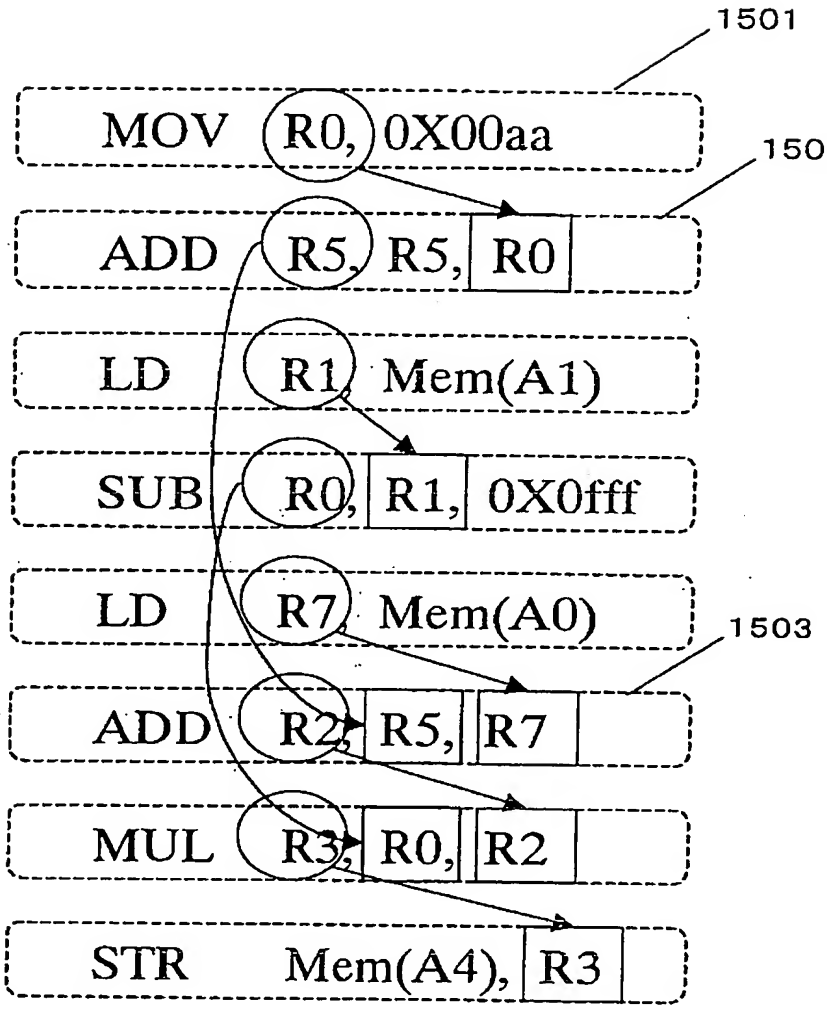
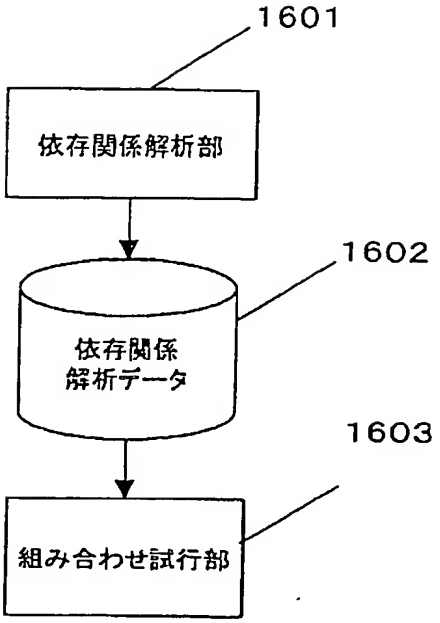

1501
MOV R0, 0X00aa
1502
ADD R5, R5, R0
LD R1, Mem(A1)
SUB R0, R1, 0X0fff
LD R7, Mem(A0)
1503
ADD R2, R5, R7
MUL R3, R0, R2
STR Mem(A4), R3

Fig.16

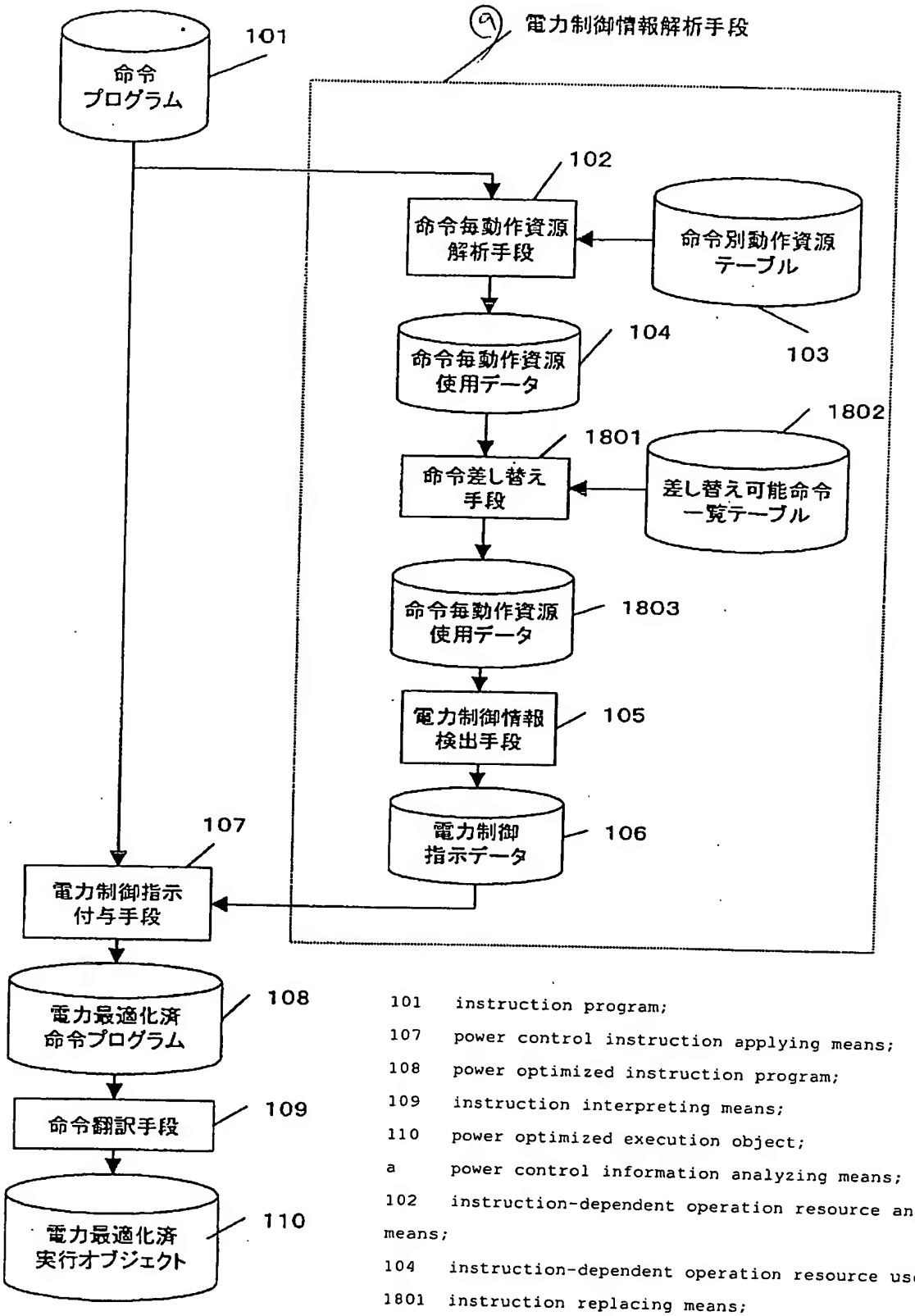


1601 dependent relationship analyzing unit;
1602 dependent relationship analysis data;
1603 combine/trial-processing unit;

Fig.17

memory Read operation;	memory Write operation;	calculator A operation;	calculator B operation;	branch unit A operation;	block A operation;	block B operation;	block C operation;	peripheral interface A operation;	parallel instruction decode unit;	data register R0 to R15;	data register R16 to R31;	address calculation unit;	threshold value unit;
LD R1, Mem(A1)	1	0	0	0	0	1	0	0	0	0	1	0	1	0
LD R7, Mem(A0)	1	0	0	0	0	1	0	0	0	0	1	0	1	0
MOV R0, 0X00aa	0	0	1	0	0	0	0	0	0	0	1	0	0	1
ADD R5, R5, R0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
SUB R0, R1, 0X0fff	0	0	1	0	0	0	0	0	0	0	1	0	0	1
ADD R2, R5, R7	0	0	1	0	0	0	0	0	0	0	0	0	0	0
MUL R3, R0, R2	0	0	0	1	0	0	0	0	0	0	1	0	0	0
STR Mem(A4), R3	0	1	0	0	0	1	1	0	0	0	1	0	1	0

Fig. 18



101 instruction program;
107 power control instruction applying means;
108 power optimized instruction program;
109 instruction interpreting means;
110 power optimized execution object;
a power control information analyzing means;
102 instruction-dependent operation resource analyzing means;
104 instruction-dependent operation resource use data;
1801 instruction replacing means;
1802 replaceable instruction list table;
1803 instruction-dependent operation resource use data;
105 power control information detecting means;
106 power control instruction data;
103 instruction-independent operation resource table;

Fig.19

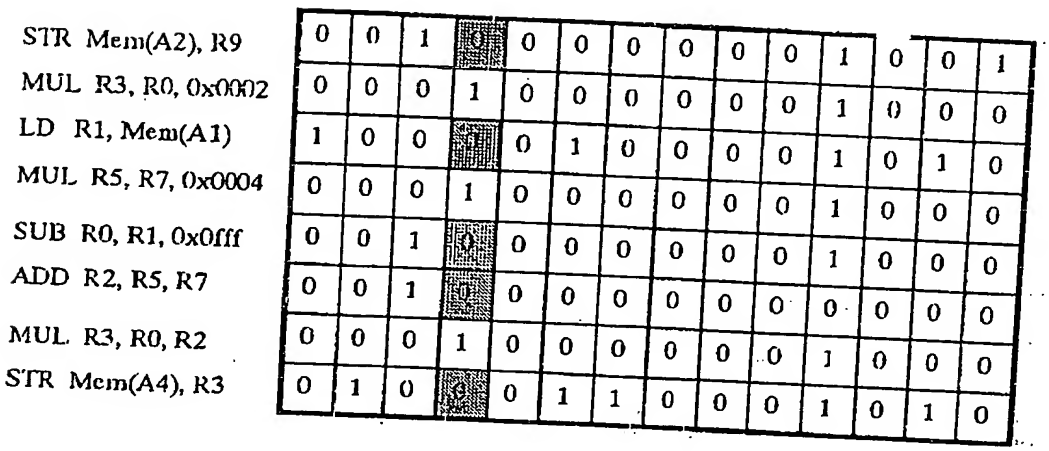

memory Read operation;
memory Write operation;
shifter operation;
multiplier operation;
branch unit A operation;
block A operation;
block B operation;
block C operation;
peripheral interface A operation;
parallel instruction decode unit;
data register R0 to R15;
data register R16 to R31;
address calculation unit;
threshold value unit;
STR Mem(A2), R9
MUL R3, R0, 0x0002
LD R1, Mem(A1)
MUL R5, R7, 0x0004
SUB R0, R1, 0x0fff
ADD R2, R5, R7
MUL R3, R0, R2
STR Mem(A4), R3

Fig.20

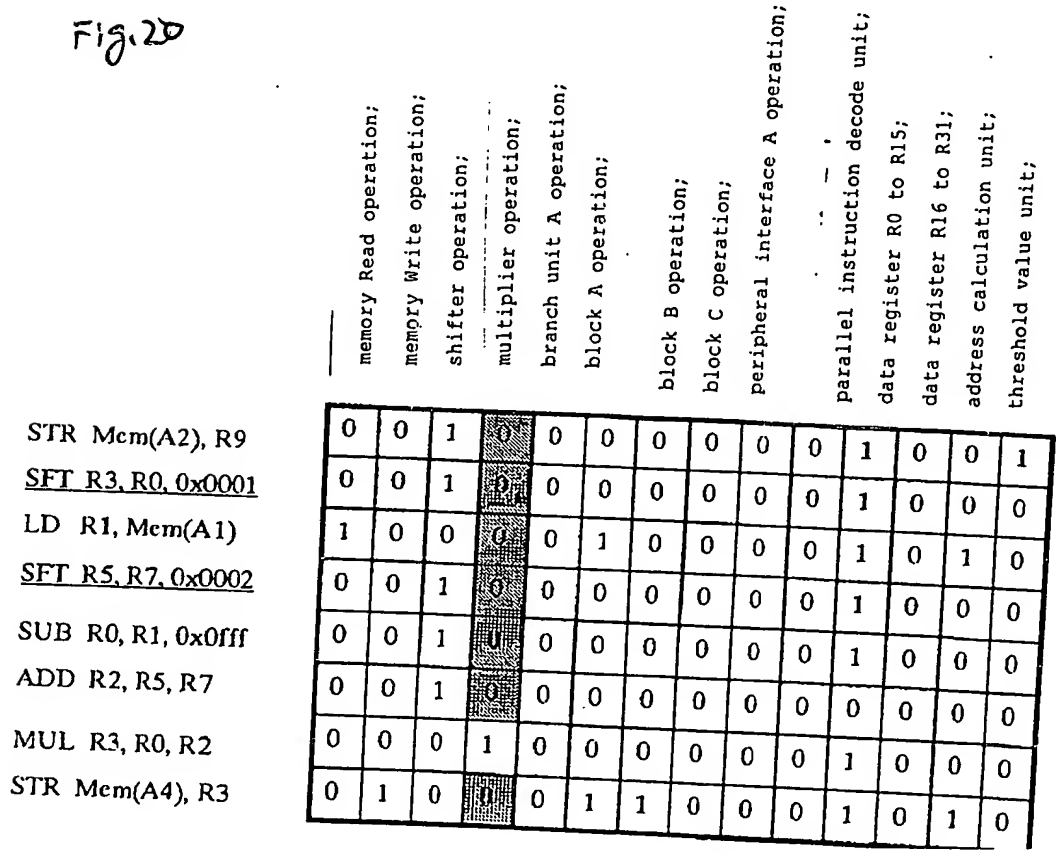
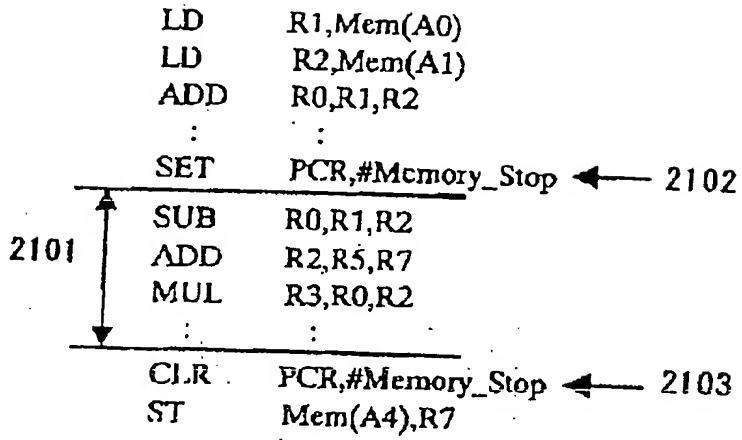

memory Read operation;
memory Write operation;
shifter operation;
multiplier operation;
branch unit A operation;
block A operation;
block B operation;
block C operation;
peripheral interface A operation;
parallel instruction decode unit;
data register R0 to R15;
data register R16 to R31;
address calculation unit;
threshold value unit;
STR Mem(A2), R9
SFT R3, R0, 0x0001
LD R1, Mem(A1)
SFT R5, R7, 0x0002
SUB R0, R1, 0x0fff
ADD R2, R5, R7
MUL R3, R0, R2
STR Mem(A4), R3

Fig-4


LD R1,Mem(A0)
LD R2,Mem(A1)
ADD R0,R1,R2
SET PCR,#Memory_Stop
2102
2101
SUB R0,R1,R2
ADD R2,R5,R7
MUL R3,R0,R2
CLR PCR,#Memory_Stop
2103
ST Mem(A4),R7